POWER MODELING METHODOLOGY FOR A PIPELINED PROCESSOR

Abstract

A method for modeling the power behavior of a pipelined processor has been developed. The method uses a power model integrated into a cycle accurate simulator. To create the power model, design blocks of the processor are divided into sub-blocks. Power modeling equations for each sub-block are developed by collaboration between the sub-block circuit designer and the simulator developer, using activity information relevant to the sub-block that is available in the simulator model. Each equation is calculated multiple times with different sets of power parameters to represent varying power conditions. Every simulation cycle, sub-block power is summed to generate full-chip power for multiple power conditions.

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